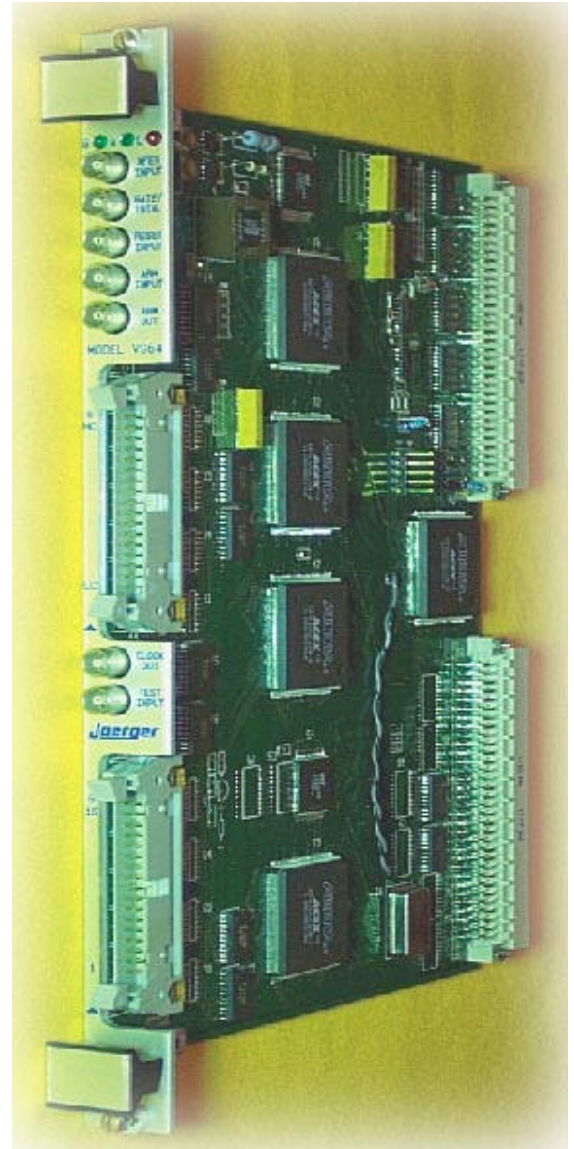


**64 CHANNEL, 32BIT 'VME' DEADTIMELESS  
100MHZ COUNTER/SCALER WITH 256K FIFO**

**FEATURES:**

- 64 CHANNELS
- 100MHZ COUNTING RATE
- DEADTIMELESS OPERATION
- $\pm 1$  LSB ACCURACY, NO PRESCALING USED
- 256K FIFO TO STORE DATA
- 32 BITS PER CHANNEL
- 24 BIT DEPTH SELECTABLE WITH CHANNEL ADDRESS, OVERFLOW, USER BIT READ
- 5 $\mu$ SECOND DWELL TIME WITH ALL 64 CHANNELS ACTIVE
- 3 MODES TO SELECT ACTIVE CHANNELS
- ALL 64 CHANNELS
- SEQUENTIALLY UP TO 64 CHANNELS
- RANDOM CHANNEL SELECTION UP TO 64 CHANNELS
- 32 CHANNEL'S WITH TTL, NIM, DIFFERENTIAL ECL COUNT INPUTS
- 64 CHANNEL'S WITH TTL INPUTS
- CONTROL INPUTS TTL VIA LEMO INPUT CONNECTORS
- COUNT INPUTS VIA FRONT PANEL LEMO OR 34 PIN RIBBON
- TTL REAR ACCESS VIA P2 CONNECTOR FOR 16 OR 32 CHANNELS
- A16/A32 D16/D32/BTL32 OPERATION
- A16 BASE ADDRESS SET WITH 5 JUMPERS
- A32 BASE ADDRESS SOFTWARE SET
- MODULE TYPE AND SERIAL NUMBER READ OUT
- WRITE TO FIFO AND CLEAR COUNTER
- WRITE TO FIFO WITHOUT CLEAR FOR ACCUMULATE MODE
- PROGRAMMABLE REFERENCE CLOCK FOR CHANNEL 1 SELECTABLE
- GLOBAL COUNT ENABLE
- FOUR COMPLETE D08(O) INTERRUPTERS:
  - INTERRUPT #1 FIFO WRITE STARTED
  - INTERRUPT #2 FIFO FULL, ERROR CONDITION FURTHER WRITES STOPPED
  - INTERRUPT #3 FIFO ALMOST FULL (HALF FULL IS OPTIONAL)



- INTERRUPT #4 CHANNEL OVERFLOW
- CONTROL INPUTS:
  - EXTERNAL LNE CLOCK, SWITCH CHANNEL COUNTER BANKS, WRITE DATA TO FIFO, NOTE: THIS CLOCK AND THE INTERNAL LNE CLOCK CAN BE PRESCALED WITH A PROGRAMMABLE 24 BIT COUNTER WHEN APPROPRIATE
  - DISABLE COUNTER, DEFAULTS TO COUNT ENABLE
  - EXTERNAL RESET
  - EXTERNAL TEST INPUT
  - USER IDENTITY BIT
- CONTROL OUTPUTS:
  - COPY TO FIFO ACTIVE, CIP
  - FIFO EMPTY
  - FIFO FULL
  - FIFO ALMOST FULL, (FIFO HALF FULL OPTIONAL)
  - PROGRAMMABLE CLOCK OUTPUT, DEFAULTS TO 10MHZ

The **JOERGER ENTERPRISES, INC.** Model VS64D is a multi-channel 6u "VME" deadtimeless 100Mhz counter. It is available with 32 or 64 channels with 32 bit capacity. Each channel contains two counter banks. While one is counting the other is loading its data into a 256k FIFO. Counting is done with no prescaling or time outs so accuracy is  $\pm 1$  lsb. To insure the maximum use of the memory and to reduce the time required in its loading the active channels can be selected. The time required by the module to load the FIFO after a LNE Clock is the number of active channels times the memory clock speed. If all 64 channels are active this time is 5 useconds. This time is also the minimum gate width that can be used. This time is available at the front panel connector as the CIP pulse. The counter bank switching may be triggered by a front panel LNE clock or internally by a programmable counter and programmable clock. The internal clock is periodic while the front panel one can be variable as the user requires. Note, Channel 1 can be set to count an internally programmed clock and could supply the user with the gate times used to acquire the data. Both the internal and external LNE signal can be prescaled with a 24 bit programmable counter. This is provided for applications that may require the counter trigger to be some sub-multiple of the LNE clock.

The module can be ordered with TTL, NIM or differential ECL inputs. It is also available with rear access from the P2 connector for 16 or 32 TTL inputs. Transfer boards that can accept high speed RS422 inputs using the new low voltage differential logic (LVDS) are available. Boards that will accept analog inputs using either V/F converters or comparators will be available shortly. Front panel data connectors can be single pin Lemo's or 34 pin ribbon connectors. For ECL systems that use TDC's or latches the input terminations are on sockets and may be removed if required.

To make maximum use of the modules capabilities a front panel reset, module disable signal and test input are provided. A user bit is also provided that can be read out either in the 24 bit data mode or as a register bit. A programmable clock output is available and is defaulted to 10Mhz. To provide system control the FIFO's empty, full and almost full flags are available.

## ***SPECIFICATIONS:***

### **COUNTER INPUTS**

TTL	Negative going TTL with 1k $\Omega$ 's to +5V
NIM	-600mv, 50 $\Omega$ 's to ground
ECL, Differential	ECL levels, terminations on sockets for removal if required

### **CONTROL INPUTS**

Trigger, LNE Clock	Negative going TTL, switch counter banks and write FIFO
Disable In	TTL low disables counting, defaults to high, counter enabled
Reset In	Negative going TTL, resets all counters, overflows, FIFO pointers, flags and control logic, (not setup registers)
Test In	Negative going TTL, clocks counters set in test mode
User Input	User supplied bit for readout with data in 24 bit mode or from register

### **CONTROL OUTPUTS**

Clock Output	Negative going TTL, continuous programmable clock, defaults to 10Mhz
CIP Out	TTL low when FIFO write is in progress
FIFO Empty	TTL low when FIFO is empty
FIFO Full	TTL low when FIFO is full, an error condition, no further writes to FIFO
FIFO Almost Full	TTL low when FIFO is 1023 words or less from full, half full optional

### **OPERATION**

Operating Speed	100Mhz, Deadtimeless
Accuracy	$\pm$ 1 LSB
Capacity	32 Bits, or 24 data bits, channel address, overflow, user bit
Memory	256K x 32 FIFO
Size	Single width, 6u, VME card
Power	+5V, (-12V with ECL or NIM input options)

STANDARD MODULE: 32 TTL CHANNELS, TWO 34 PIN RIBBON CONNECTORS, SIGNAL AND RETURN PIN PER CHANNEL

### **OPTIONS:**

- 1) 64 CHANNELS, TTL INPUTS, TWO 34 PIN RIBBON CONNECTORS
- 2) NIM SIGNAL INPUTS, 32 CHANNELS
- 3) DIFFERENTIAL ECL INPUTS, 32 CHANNELS, 34 PIN RIBBON CONNECTOR
- 4) REAR P2 ACCESS, TTL INPUTS, 32 CHANNELS



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