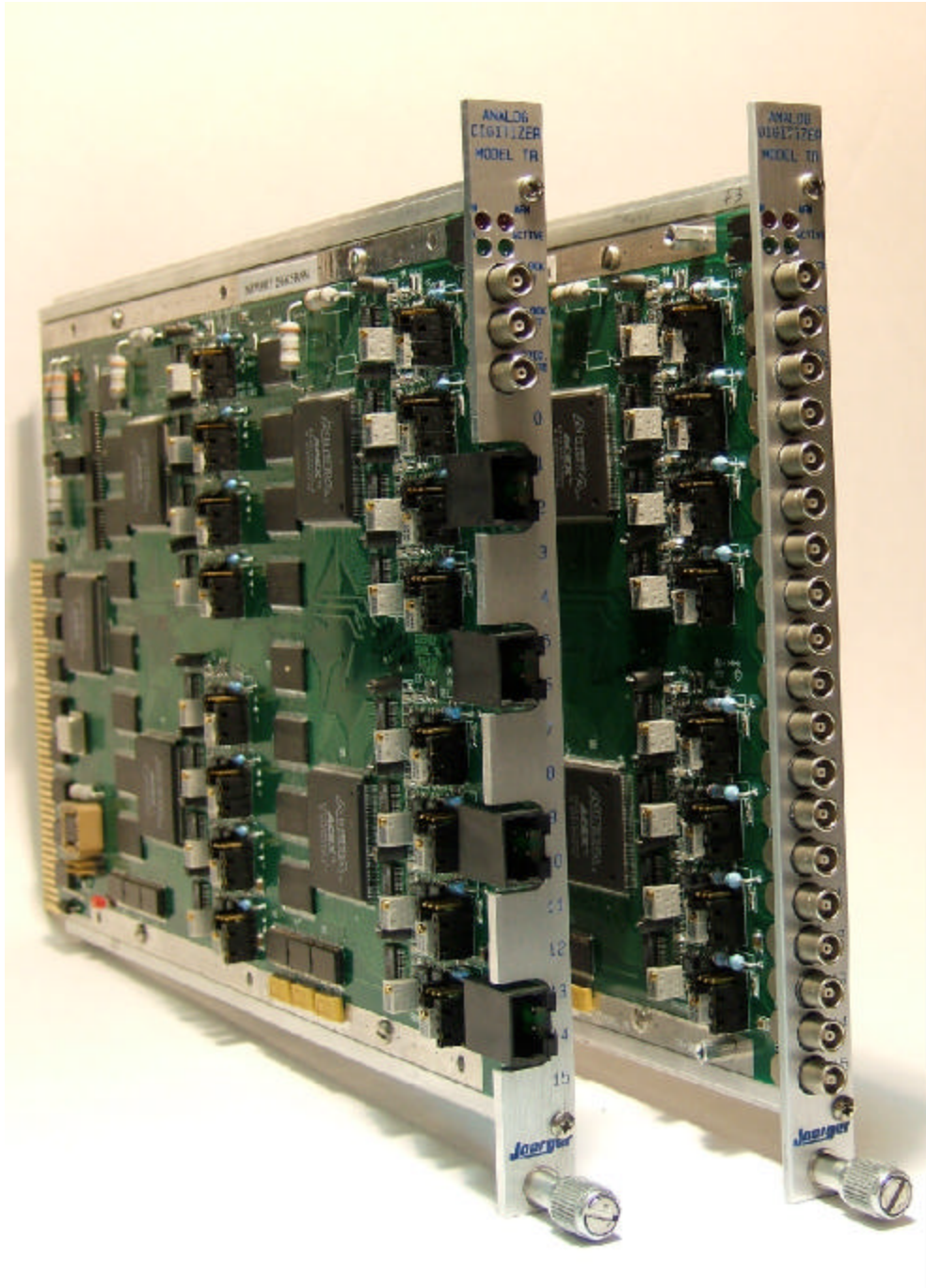


**“CAMAC” 16 INDIVIDUAL, 40MHZ, 12 BIT,
ANALOG DIGITIZERS**



FEATURES:

- 16 INDIVIDUAL ANALOG DIGITIZER CHANNELS
- AVAILABLE IN SINGLE WIDTH "CAMAC" MODULE
- CLOCK SPEEDS, 10MHZ or 40MHZ
- RESOLUTION, 12 BITS
- SIGNAL AVERAGING FOR IMPROVED SIGNAL TO NOISE RESPONSE
- "IMPROVED" MEMORY UP TO 512KWORD OF STATIC RAM PER CHANNEL, 8MWORDS TOTAL
- SINGLE ENDED OR DIFFERENTIAL INPUTS, JUMPER SELECTABLE
- 100KOHM INPUT IMPEDANCE, DC COUPLED
- 50 OHMS FOR SINGLE ENDED APPLICATIONS OR 100 OHMS FOR DIFFERENTIAL APPLICATIONS, JUMPER SELECTABLE
- 40MHZ AMPLIFIER BANDWIDTH FOR GOOD HIGH FREQUENCY DATA RETENTION
- SINGLE ENDED INPUT MODE CAN BE OFFSET FULL SCALE FOR IMPROVED RANGE
- ± 5 VOLT INPUT RANGE
- EXTERNAL CLOCK INPUT
- EXTERNAL CLOCK OUTPUT
- EXTERNAL TRIGGER / GATE INPUT
- GATING AND TRIGGERING AVAILABLE USING FRONT PANEL INPUT SIGNALS, THRESHOLDS AND POLARITY SELECTABLE
- VALID DATA CAPABILITY, EACH CHANNEL'S MINIMUM SIGNAL REQUIREMENT ARE LOADED AND WHEN EXCEEDED A VALID DATA BIT IS SET FOR THAT CHANNEL
- POST, MULTI-POST, PRE/POST AND MULTI-PRE/POST TRIGGERING AVAILABLE
- ALL TRIGGER ADDRESSES ARE STORED TO FACILITATE READ OUT
- 12, 24 OR 48 BITS CAN BE READ OUT WITH NORMAL READ, "FASTCAMAC" LEVEL 1 OR LEVEL 2 MODES
- FIELD PROGRAMMABLE GATE ARRAY'S ARE USED FOR ALL INTERNAL LOGIC
- AT POWER UP THE MODULE IS SET WITH A SOCKET MOUNTED CONFIGURATION CHIP
- TO HANDLE UNIQUE CUSTOMER REQUIREMENTS THE CONFIGURATION CHIP IS RE-PROGRAMMABLE
- EXTERNAL AND INTERNAL CRYSTAL CLOCK SPEEDS ARE PROGRAMMABLE
- ACTIVE MEMORY SIZE IS BIT SELECTABLE
- POST TRIGGER LENGTH IS BIT SELECTABLE
- TO MONITOR MULTIPLE TRIGGER EVENTS A REAL TIME CLOCK IS PROVIDED WHICH IS STARTED WITH ARM AND ITS CLOCK RATE IS PROGRAMMABLY SELECTED
- MODULE TYPE AND SERIAL NUMBER ARE PROVIDED FOR IDENTIFICATION AND CALIBRATION
- ADC PIPE LINE DELAYS ARE HANDLED INTERNALLY AND ARE INVISIBLE TO THE USER
- TWO SOFTWARE SYSTEMS ARE AVAILABLE AT NO CHARGE. THEY ARE "LABVIEW" AND MDSplus, A DATA ACQUISITION SYSTEM DEVELOPED AT MIT

JOERGER ENTERPRISES, INC. has designed the Model TR as a versatile analog digitizer for CAMAC users. While few new CAMAC systems are being set up there are 1000's of CAMAC crates and systems still being used. This new module features the latest amplifiers and ADC's available with all the logic done with field programmable logic chips. Surface mounted components have been used, providing an improvement in performance, capacity and lower channel costs. The module contains 16 individual channels. The input connectors are Lemo. The maximum clock speeds available are 10Mhz and 40Mhz. To provide the user a great degree of freedom in input capability the module is laid out to accept either single ended inputs or differential inputs. The input type is user selectable with jumpers. The input is 100Kohm and is DC coupled. The bandwidth is 40 Mhz to insure good waveform recording. When a situation requires a lower input impedance, jumpers are provided. The terminating resistors for single ended inputs is 50 ohms, ½ watt and the differential inputs is 100 ohms, ¼ watt. To extend the range for single ended inputs a full scale offset pot is provided. The input range is ± 5 volts. The analog power and ground for each channel is filtered. This lowers the channel noise and improves channel cross talk. The ADC's resolution is 12 bits and signal averaging is provided for improved signal to noise performance. Averaging allows the ADC to run at the maximum rate, it's output is averaged to the level requested and the result loaded into memory.

The use of field programmable gate array's (FPGA) allows a great many features to be provided. To simplify module use it is reset with these features disabled. This leaves the user with the ability to select which ones would best serve the application. Data can be read out 12 or 24 bits at a time in either standard mode or "FASTCAMAC" level 1 mode. All data is read from the selected channel simplifying data taking. Because there is a large amount of data present a valid data mode is provided. This allows each channel to be loaded with a minimum data level. During conversion the ADC's output is compared to this minimum level and if it is exceeded a bit for that channel is set. At the end of the cycle the valid data word can be read out and only channels with valid data need be read.

Versatile triggering and gating is provided. A cycle can be triggered with a CAMAC command, an external positive input, which can be programmed as either a trigger or gate signal and from a channel's input signal. Each channel can set a threshold and a direction bit. One or more channels can be enabled and the start signals are or'ed to control the cycle

The module can operate in post, multi-post, pre/post and multi-pre/post trigger modes. To facilitate read out all trigger addresses are recorded. In addition, a real time counter is provided that is started when the module is armed, counts at a programmable selected clock, stores the arrival of each trigger and provides the real time each trigger was received. The active memory size and the post trigger size can be bit selected up to the maximum size of the memory. This provides the user maximum control over data acquisition. The memory can be programmed to cycle once and stop or over write itself. The module is available with either 256kwords or 512kwords of Static RAM per channel. To handle larger memory requirements an ADC may be programmed to drive either 2 or 4 adjacent channel's memory. This can provide a channel with up to 2Mword of memory. The module is programmed for memory sharing. Static memory is used to insure excellent acquisition of real time signals. Memory updating is not required avoiding dead spots. Two additional features are provided in the trigger circuit. In pre trigger mode a minimum number of clocks can be set before a trigger will be accepted. This insures a specified number of pre-trigger data is recorded before the post trigger count down is started. The second feature provides the ability to delay the active cycle after the receipt of a trigger by a programmable number of clock signals.

A standard module is 10Mhz, 256kwords of memory, ± 5 volt input, Lemo connectors.

CAMAC COMMANDS

F _A	Q	X	FUNCTION
0 ₁	1	1	Read Control Register (see tables that follow for specs)
0 ₂	1	1	Read Clock Setup Register
0 ₃	1	1	Read Post Trig Size Register
0 ₄	1	1	Read Minimum PreTrigger Sample Register (# of PreTrigger samples before a Trigger is accepted)
0 ₅	1	1	Read Trigger Delay Register
0 ₆	1	1	Read Averaging Setup Register
0 ₇	1	1	Read LAM Setup Register
0 ₈	1	1	Read Real Time Clock Setup Register
0 ₉	1	1	Read Memory Address Pointer
0 ₁₀	1	1	Read Multi Pre/Post Setup Register
0 ₁₁	1	1	Read Event Register (# of post trigger events for Disarm and/or interrupt)
0 ₁₅	1	1	Read Module ID and Serial Number
1 ₀	1	1	Read Status Register
1 ₂	1	1	Read Valid Data Register, all 16 channels (1 bit / ch)
1 ₃	1	1	Read Valid Trigger Register, all 16 channels (1 bit / ch)
1 ₄	1	1	Read Trigger generation channel participation enable register
1 ₅	1	1	Read Completed Post Trigger Cycles Counter Register (stored on disarm)
1 ₆	1	1	Read Completed Post Trigger Cycles Counter
1 ₇	1	1	Read Trigger Counter Register (stored on disarm)
1 ₈	1	1	Read Trigger Counter (only valid if RTC is enabled)
1 ₉	1	1	Read Real Time Counter high 2bytes
1 ₁₀	1	1	Read Real Time Counter low 2bytes
			'on the fly' readout not protected from readout errors & low and high may be from different times. For Reference Only.
1 ₁₄	valid	1	Read Last Address for each complete Post Trigger Cycle (read up to 255 times for 255 Addresses) 9 ₈ will initialize readout to 1st stored address
1 ₁₅	valid	1	Read Real Time Counter Value for each Trigger (from memory) High byte first using R1-16 (read up to 510 times for 255 Triggers) 9 ₉ will initialize readout to 1st stored value
2 ₍₀₋₁₅₎	valid	1	Read sample data from memory using selected data width of 12 or 24 bits (see Control Reg) Enable Readout with F17A1 If Wrap=0, no Q at Memory Overflow
3 ₍₀₋₁₅₎	1	1	Read Last Conversion register for ch 1-16
4 ₍₀₋₁₅₎	1	1	Read Valid Data Comparator Threshold register for ch 1-16

F_A	Q	X	FUNCTION
5 ₍₀₋₁₅₎	valid	1	Level 1, FastCamac Read sample data from memory using selected data width of 12, 24 or 48 bits. Enable Readout with F17A1 If Wrap=0, no Q at Memory Overflow
6 ₍₀₋₁₅₎	1	1	Read Trigger Threshold / Setup register for ch 1-16
8 ₍₀₋₃₎	lam	1	Test LAM's
9 ₀	1	1	Master reset
9 ₂	d	1	Reset Memory Location Counter to zero (beginning of memory)
9 ₆	d	1	Reset Completed Post Trigger Cycles Counter
9 ₈	d	1	Initialize pointer for Read Last Address for each complete Post Trigger Cycle (1 ₁₄) to 1st stored address
9 ₉	d	1	Initialize pointer for Read Real Time Counter Value for each Trigger (1 ₁₅) to 1st stored address
10 ₀	1	1	Resets LAM FF
16 ₁	d	1	Write Control register
16 ₂	d	1	Write Clock Setup Register
16 ₃	d	1	Write Post Trig Size Register
16 ₄	d	1	Write Minimum Pre Trigger Sample Register
16 ₅	d	1	Write Trigger Delay Register
16 ₆	d	1	Write Averaging Setup Register
16 ₇	d	1	Write LAM Setup Register
16 ₈	d	1	Write Real Time Clock Setup Register
16 ₉	d	1	Write Memory Address Pointer (not for Readout)
16 ₁₀	d	1	Write Multi Pre/Post Setup Register
16 ₁₁	d	1	Write Event Register (# of post trigger events for Disarm and/or interrupt)
17 ₁	d	1	Set module to Read mode, preset readout address pointer with data on W1-W18
17 ₂	d	1	Write Valid Data Comparator Threshold register for ALL Channels
17 ₃	d	1	Write Trigger Threshold / Setup register for ALL Channels
17 ₄	d	1	Write Trigger generation channel participation enable register
20 ₍₀₋₁₅₎	d	1	Write Valid Data Comparator Threshold register for Ch 1-16
21 ₁	1	1	Clear all channels Valid Data Flags
21 ₂	1	1	Clear all channels Internal Trigger Generator Flags
22 ₍₀₋₁₅₎	d	1	Write Trigger Threshold / Setup register for ch 1-16

F_A	Q	X	FUNCTION
24 ₀	1	1	Disables LAM response
25 ₀	1	1	Arm module for a digitizing cycle (Start)
25 ₁	a	1	Internal Trigger (Stop)
25 ₂	1	1	Abort (clear arm, clear active, stop digitizing, disable readout mode)
26 ₀	1	1	Enables LAM response
27 ₍₀₋₃₎	ls	1	Tests LAM Source FF's
Z(S2)			Reprogram module like power-up (front panel Arm & L lights will flash)

a	Q=1 if armed
d	Q=1 if not armed
valid	Q=1 for valid data, Q=0 for last word +1
lam	Q=1 if LAM=1
ls	Q=1 if LAM Source=1

OPTIONS:

1	10Mhz clock with 512kwords of Static RAM per channel
2	40Mhz clock, 512kwords of Static RAM per channel

POWER CONSUMPTION(while active):

+ 6 VOLTS	2.5A, 10Mhz, 3.0A, 40Mhz
+ 24 VOLTS	150ma
- 24 VOLTS	400ma

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