

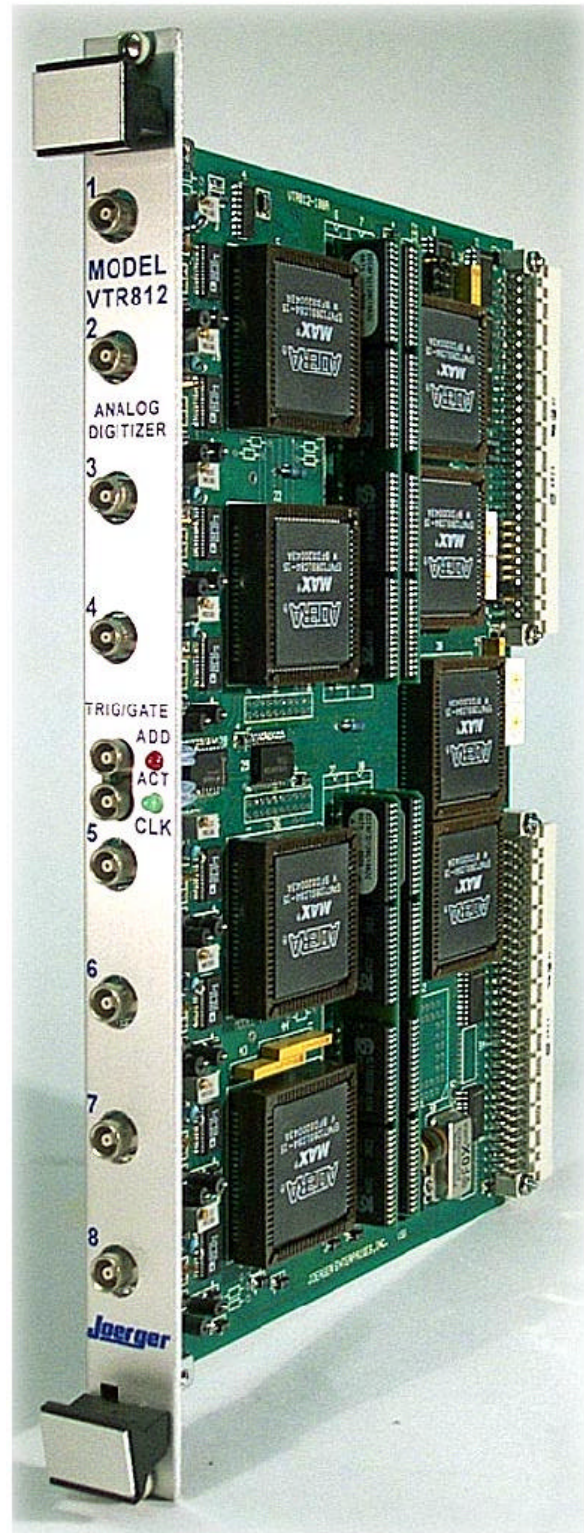
EIGHT CHANNEL, 40 MHZ, 12 BIT “VME” ANALOG DIGITIZER WITH 8M WORD SRAM

FEATURES:

- 4 OR 8, INDEPENDENT, 40 MHZ, 12 BIT ANALOG DIGITIZERS
- 1M SAMPLES OF SRAM PER CHANNEL, 8M SAMPLES TOTAL
- PROGRAMMABLY SELECTABLE FOR 4 CHANNEL OPERATION WITH 2MSAMPLES OF SRAM PER CHANNEL
- WIDE INPUT BANDWIDTH FOR GOOD WAVEFORM TRACKING
- HIGH NOISE IMMUNITY AND LOW CHANNEL CROSSTALK
- REAL TIME READ OUT OF ADC DATA IN ACTIVE MODE
- HIGH SPEED READOUT, 2 CHANNELS PER READ
- PRE/POST & MULTIPLE PRE/POST TRIGGER RECORDING WITH ADDRESS LOCATIONS INTERNALLY STORED TO FACILITATE DATA READ OUT
- POST AND MULTIPLE POST TRIGGER RECORDING
- PROGRAMMABLE INTERNAL CRYSTAL CLOCK OR EXTERNAL CLOCK
- HIGH COMMON MODE REJECTION
- INTERRUPT STRUCTURE
- BLOCK TRANSFER MODE D32:BLT
- “LABVIEW” & “EPICS” SOFTWARE AVAILABLE

APPLICATIONS:

- HIGH SPEED, ACCURATE, ANALOG TO DIGITAL RECORDING
- REAL TIME DIGITAL RECORDING OF ANALOG SIGNALS
- “OSCILLOSCOPES”, USING ITS HIGH IMPEDANCE AND MEMORY PROVIDES FAST ACCURATE RECORDING AND TROUBLE SHOOTING OF ANALOG DATA



The JOERGER ENTERPRISES, INC. MODEL VTR812 is available with 4 or 8 individual, 12 bit analog digitizers in a 6U, VME module. The **Model VTR812/40** operates at 40Mhz and the **Model VTR812/10** operates at a clock speed of 10Mhz. It is completely self contained and can store 1M samples of data per channel in SRAM, 8M samples total in a single width. When additional memory is required the module may be programmably set to operate two memory banks from one ADC providing 2M samples of data for that channel. To insure the highest performance the ADC is driven with an offset, differential input. A wide band, differential input/output amplifier with an output offset capability designed specifically for this type ADC is used. The differential inputs are buffered providing the module either single ended or differential inputs with an input impedance of over 10M Ω 's. This balances the module in either mode and for single ended inputs the return line is grounded internally. When lower impedance's are required an on board jumper is provided for each channel. For single ended inputs the impedance is 50 Ω 's and for differential inputs 100 Ω 's is provided. Other impedance's can be provided.

Its high input impedance and large memory allows it to be used in place of an oscilloscope for both analog monitoring and trouble shooting. When looking for problems even in slow speed systems it provides a complete picture of the event.

Each channel accepts an analog signal, digitizes it using a programmable internal crystal clock or an external clock and loads the data into its SRAM. To interface the ADC's output, high speed PLD's are used. In addition to writing the memory and gating the data for readout the active ADC's data is also latched and available for real time readout over the VME bus while the module is recording. The "active" data is also available from the P2 connector. Allowing the user the ability to monitor the ADC's output provides a wide possibility for uses in system operation. To insure high speed readout each module is read out 2 channels at a time on 32 data lines.

The addressing, address control, ADC interface, VME logic and commands are all done with high speed PLD's. The analog inputs have been designed to handle a wide variety of signals. Special care in the layout and filtering provide both low channel cross talk and low noise, often a problem with multi-channel analog input modules. When an application requires filtering, external filters are recommended. All channels use a common clock and control signal's and operate simultaneously.

Each channel's data is in a contiguous block of memory with the module's base address selected by switches. The three control and status registers are accessed via short addressing to a 256 byte block. The control register selects the operating parameters for the module. The gate duration register contains the number of samples to be taken after a trigger. The location register contains the pointer to the next memory address to be filled with data. In addition to controlling the module with registers it can be Triggered, Disarmed and the memory location can be reset with separate commands without data. To simplify system implementation "LABVIEW" and "EPICS" software is available.

To add flexibility the module may be operated in several modes. Post trigger, multiple post trigger, pre/post trigger and multiple pre/post trigger operations can be selected. To facilitate data readout the stop address is recorded in all modes and the number of valid cycles is recorded and can be readout. In multiple pre/post trigger the memory can be divided in up to 16 equal sections. Each section runs a normal pre/post trigger cycle and records that sections stop address in memory so data for that section can be read. This is repeated for each trigger and stops when the memory is full.

The external TRIGGER/GATE input allows the module to use this signal as a trigger or gate signal and is selected in software. When GATE is selected this determines the cycle gate time. If TRIGGER is selected the gate time is set by the internal gate duration register. In TRIGGER mode the post trigger

cycle starts digitizing on receipt of a trigger, takes the number of samples set by the gate duration register, stops and sets an interrupt. If the Auto Reset is on, the next trigger will reset the location counter to zero and overwrite the previous samples. For multiple post trigger operation, Auto Reset is turned off and each following trigger will not reset the location counter and the samples will be stored sequentially until the memory is full. If the "Memory Wrap" mode is off, and the cycle is complete, an interrupt is set and further triggers are ignored. If the Wrap mode is on, when the memory fills, it will start overwriting the memory and accept triggers until the module is disarmed. In the pre/post trigger mode the module starts taking data when the unit is armed and cycles through the memory overwriting old data. Upon receipt of a trigger the module takes the number of samples set by the duration counter, stops and sets an interrupt. The complete memory is used with the post trigger samples preset by the gate duration. The balance of the memory contains pre trigger information. If GATE is selected its pulse width will determine the gate times.

SPECIFICATIONS

ANALOG INPUT	±2 Volts, single ended standard, differential input optional
INPUT IMPEDANCE	10 MΩ's, jumper selectable to 50Ω's, other impedance's optional
COMMON MODE REJECTION	-70dB min., DC to 500khz
CHANNEL CROSSTALK	-66dB min. at 10Mhz input rate
BANDWIDTH	VTR812/10, 10Mhz Minimum VTR812/40, 40Mhz Minimum
ACCURACY	. .05% typical
DIFFERENTIAL LINEARITY	±.3LSB, Typ., No missing codes
CONVERSION RATE	VTR812/10, 10Mhz maximum, VTR812/40 40Mhz maximum, selected from 8 scaled frequencies using either the SYS Clock, on board crystal oscillator or an external clock.
RESOLUTION	12 Bits.
MEMORY	128K samples/channel Standard, 512K, 1M samples/channel Optional. Note: module may be set to 4 channel mode doubling the memory per channel
TRIGGER/GATE INPUT	TTL Level, trigger or gate mode internally selectable
CLOCK INPUT	TTL Level
VME INTERFACE	D8 (EO), D32, D32:BLT, A16, A32 SLAVE
CONTROL/STATUS REGISTERS	Read/Write: select clock rate, disarm at cycle completion, bus trigger, external clock, external trigger, external gate, reset on trigger, wrap, post, pre/post and multiple pre/post trigger modes, arm, active, set to 4 channel mode, last channel read
GATE DURATION REGISTER	Read/Write: select the number of conversions to perform after a trigger.
LOCATION REGISTER	Read/Write: a pointer to the next sample location
INTERRUPT ID REGISTER	Read/Write Status/ID word
IRQ LEVEL REGISTER	Read IRQ level jumpers
SYSRESET, INT. RESET	Resets module and control register, aborts recording cycle
SOFTWARE	"LABVIEW" and "EPICS" software is available
POWER REQUIREMENTS:	+5V, -12V, 13 watts total
SIZE:	Single width "VME" 6U card

CONNECTORS: TRIGGER/GATE, CLOCK; LEMO ERA 00.250
SINGLE ENDED INPUTS; LEMO ERA 00.250
DIFFERENTIAL INPUTS; LEMO ERA 0S.302

OPTIONS:

- 1) MODEL VTR812/10, 10Mhz speed
- 2) MODEL VTR812/40, 40Mhz speed
- 3) 512K SRAM per channel
- 4) 1M SRAM per channel
- 5) Multiple pre/post trigger
- 6) Differential inputs
- 7) Active read out of channels 5-8 on P2
- 8) 4 channel's
- 9) 8 channel's

JEI0203

PLEASE NOTE: When choosing an analog input module many factors should be considered. It is recommended reading "SELECTING AN ANALOG INPUT MODULE" on our web site: www.joergerinc.com , under "What's New"



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