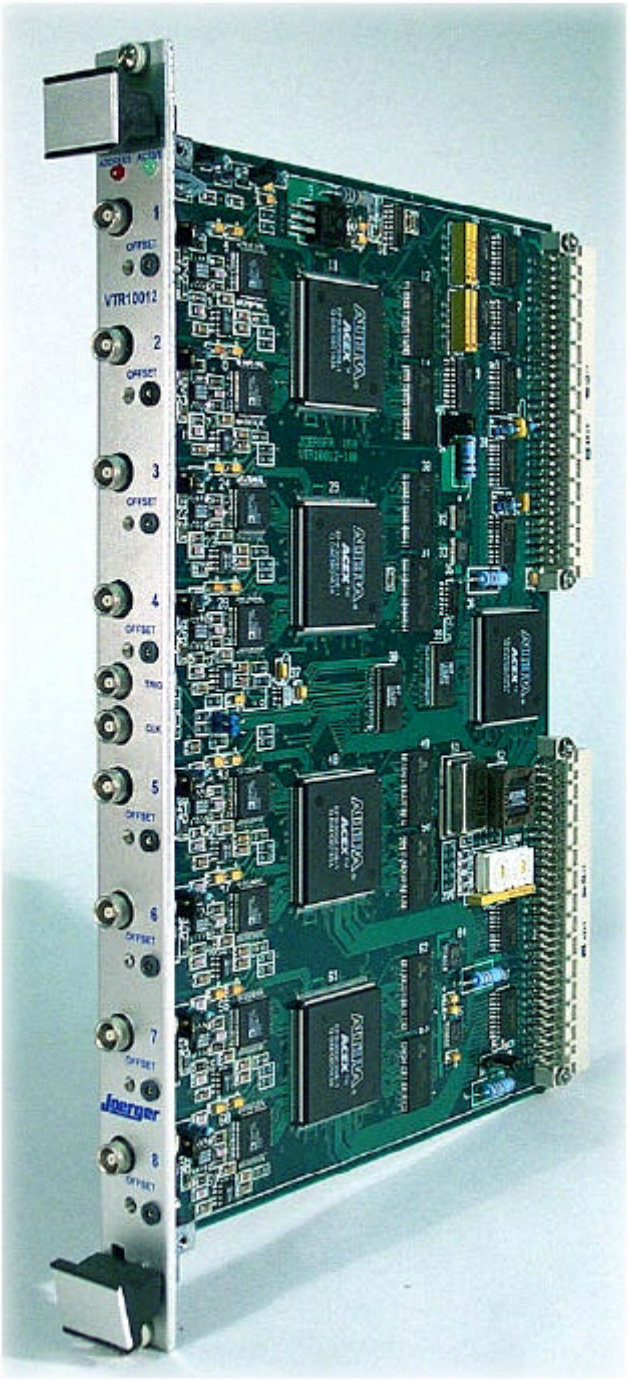
Joerger ENTERPRISES, INC.

MODEL VTR10012

EIGHT CHANNEL, 100 MHZ, 12 BIT "VME" TRANSIENT RECORDER WITH 2M SAMPLE SRAM

FEATURES:



- EIGHT INDIVIDUAL, 100 MHZ, 12 BIT TRANSIENT RECORDER CHANNELS
- 256K SAMPLES OF SRAM PER CHANNEL, 2M SAMPLES TOTAL
- RECORDING MODES:
  POST TRIGGER
  MULTIPLE POST TRIGGER
  PRE/POST TRIGGER
  MULTIPLE PRE/POST TRIGGER
- DATA CAN BE READ AT ANY TIME, WHETHER THE CHANNEL IS ACTIVE OR NOT, ALLOWING DATA VERIFICATION OR CHANNEL OFFSET OR GAIN TESTS
- FRONT PANEL, REAL TIME DATA, AVAILABLE AT 100MHZ VIA A STANDARD VITA FPDP CONNECTOR, MODEL VTR10012-FP
- ALL TRIGGER ADDRESSES STORED TO FACILITATE DATA READOUT
- REAL TIME TRIGGER ADDRESSING IN MULTIPLE TRIGGER MODES VIA AN ADDITIONAL 32 BIT REAL TIME COUNTER
- HIGH INPUT IMPEDANCE, 10 MΩ's, JUMPABLE TO 50Ω's WHEN REQUIRED
- BIPOLAR OR UNIPOLAR INPUTS USING FULL SCALE OFFSET CONTROL
- SINGLE ENDED OR DIFFERENTIAL INPUTS
- HIGH GAIN STABILITY WITH LOW DRIFT VOLTAGE REFERENCE FOR ALL CHANNELS
- WIDE INPUT BANDWIDTH FOR GOOD WAVEFORM TRACKING
- INDIVIDUAL FILTERING OF EACH CHANNELS ANALOG SUPPLIES AND GROUNDS, PROVIDING HIGH NOISE IMMUNITY AND LOW CHANNEL CROSSTALK
- **"SPARSE"** SCAN MODE FOR IMPROVED READOUT SPEED

- HIGH SPEED READOUT, 2 CHANNELS PER READ
- ACTIVE TRIGGER CAN BE DELAYED FROM TRIGGER SIGNAL, PROGRAMMABLE
- INTERNAL CRYSTAL CLOCK OR EXTERNAL CLOCK, PROGRAMMABLE
- INTERRUPT STRUCTURE
- BLOCK TRANSFER MODE
- LOW POWER CONSUMPTION, 13 WATTS TOTAL AT 100MHZ, GREATLY IMPROVING CRATE COOLING AND MODULE RELIABILITY
- **"EPICS"** SOFTWARE AVAILABLE
- LOW COST 1K SAMPLE PER CHANNEL FOR HIGH RESOLUTION AND SMALL DATA RATE APPLICATIONS, MODEL VTR10012-8

APPLICATIONS:

- HIGH SPEED, ACCURATE, ANALOG DIGITATION
- REAL TIME DIGITAL RECORDING OF ANALOG SIGNALS
- OSCILLOSCOPES, USING ITS HIGH IMPEDANCE AND MEMORY PROVIDES FAST ACCURATE RECORDING AND TROUBLE SHOOTING OF ANALOG DATA
- COMMUNICATIONS, USING THE REAL TIME ADC OUTPUT
- RADAR AND SATELLITE SYSTEMS

The JOERGER ENTERPRISES, INC. MODEL VTR10012 contains eight, 100Mhz, 12 bit transient recorders in a 6U, VME module. High resolution and accuracy have been attained with the use of ADC's designed to run at 100Mhz with 12 bit resolution. This avoids the many problems encountered when lower speed ADC's are coupled to provide higher overall speed operation. Each channel is completely self contained and can store up to 256k samples per channel of data in SRAM, 2M total in a single width module. The latest ADC's, amplifiers, memory and the use of high speed programmable logic devices makes all these features possible. While many high speed modules require a great deal of power, the VTR10012 uses only 13 watts while running at 100Mhz. This is often an important consideration when many of these may be used in a single crate. The ADC uses a pipeline converter. This delay is taken care of internally and is invisible to the user. For 100Mhz applications were the data rate is small the Model VTR10012-8 offers a low cost option with 1k samples per channel.

To insure high performance each channel contains a wide bandwidth amplifier section. To provide good ADC performance it is driven with an amplifier with a differential output which is internally offset to provide an input designed especially for these latest type converters. The amplifier also has a differential input which is buffered by two voltage followers. This isolates the ADC and provided a 10MΩ input impedance. This provides either a single ended input or a true differential input. The high input impedance affords the ability to monitor an input signal without loading it down. This type input coupled with its large memory provides the ability to monitor a wave shape over a long period of time. Even when trouble shooting a slow speed system it provides a high speed, high-resolution picture. A difficult feature to accomplish with an analog oscilloscope. When required a lower input impedance can be selected with an on board jumper.

Each channel accepts a 2 volt analog signal. On single ended inputs full scale offset is provided by a front panel potentiometer. This allows either bipolar or unipolar input ranges. A test point is included to monitor the offset. The offset can also be readout on the VME bus and provides the ability to set the overall offset and to monitor each channels gain. Gain stability is enhanced through the use of a separate, high accuracy, high temperature stability, voltage reference for the ADC's. The input is digitized using a programmable internal crystal oscillator or an external clock and loads the data into its internal SRAM. To insure high-speed readout, data is read out 2 channels at a time on 32 data lines. To increase overall data readout speed a "SPARSE" scan mode is provided. Each channel has a 12 bit register that can be set with a minimum input level. Its output is compared to the converted input level and if it is not exceeded the data is considered invalid. This valid data word can be read out indicating which channels should be read. All channels use a common clock, address, control signals and operate simultaneously. Special care has been extended to insure the trigger and addresses are matched in time.

The analog inputs have been designed to handle a wide variety of signals. Each channels analog power and analog ground are individually filtered. This special care in the layout and filtering provide both low channel cross talk and low noise, often a problem with multi-channel analog input modules. When an application requires filtering, external filters are recommended.

Control and status registers are accessed via short addressing. The control registers select the operating parameters for the module. The gate duration register contains the number of samples to be taken after a trigger.

To facilitate data readout two address memories are provided. One records the memory address at the end of each cycle. The second memory records the time each trigger was received and is taken from the real time counter. It is 32 bits long and starts when a cycle has begun. A trigger counter is provided to record the number of complete triggers cycles received. This information allows the user the ability to know how many triggers were received, their address in memory and the time the triggers were received.

For applications that require 100Mhz resolution, but need a minimum of data recorded, a low cost option is available, the Model VTR10012-8. Its has an on board SRAM memory of 1ksamples per channel and operates in post trigger mode.

When a larger memory is needed, or other recording options required, the Model VTR10012 is recommended. It can operate in post trigger, multiple post trigger, pre/post and multiple pre/post trigger modes. The post trigger mode starts digitizing on receipt of a trigger, takes the number of samples set by the gate duration register then stops and sets an interrupt. If Auto Reset is on, the next trigger will reset the location counter to zero and overwrite the previous samples. For multiple post trigger operation, Auto Reset is turned off and each following trigger will not reset the location counter and the samples will be stored sequentially until the memory is full. To account for the timing in multiple trigger operations a 32 bit counter is provided that records the time each trigger is received and stores it in memory. This can be readout along with the number of triggers received. If the "Memory Wrap" mode is off and the cycle is complete, an interrupt is set and further triggers are ignored. If the Wrap mode is on, when the memory fills it will start overwriting the memory and accept triggers until the module is disarmed.

In the pre/post trigger mode the module starts taking data when the unit is armed and cycles through the memory overwriting old data. Upon receipt of a trigger the module takes the number of samples set by the gate duration register, stops and sets an interrupt. The complete memory is used with the post trigger samples preset by the gate duration. The balance of the memory contains pre-trigger information. For multiple pre/post trigger operation the memory is divided programmably into sections of up to 16. Now each section operates as a pre/post trigger cycle with each memory address stored, the real time of each trigger stored and the number of triggers. At the completion of operation an interrupt is set. This then provides the user a complete picture of the data recorded, the memory addresses, the time the triggers were received and the number of triggers.

All recording cycles are triggered, either internally or externally. As an added feature this trigger can be delayed digitally by programmable setting of a counter and its clock speed. This could prove useful in operations where there is a time gap when the trigger appears and active recording should begin.

To make the module more useful it may be read out while active or idle without disrupting the operation. This allows the data from the ADC to be monitored while active. It also provides the ability to operate the module as an ADC or to check each channel's offset and gain.

If real time ADC data is required at speeds to 100Mhz the Model VTR10012-FP is available. This module contains 4 channels and the ADC data is available from the front panel. It uses the Vita standard FPDP connector. It is useful when the data can be used in system operations like communications. A separate data sheet is available on this module.

To simplify system implementation "EPICS " software is available.

SPECIFICATIONS (per channel)

ANALOG INPUT	±1 Volt, single ended, Differential input optional
INPUT OFFSET ADJUST	Full scale front panel input offset adjustment and test point
GAIN STABILITY	7ppm/ °C
INPUT IMPEDANCE	10 MΩ's, jumper selectable to 50Ω's, other impedance's optional
CHANNEL CROSSTALK	<1 LSB typical at 10Mhz input rate
BANDWIDTH	100Mhz Minimum
DIFFERENTIAL LINEARITY	±.3LSB, Typ., No missing codes
CONVERSION RATE	100Mhz max., programmable using either the on board crystal oscillator or an external clock.
RESOLUTION	12 Bits.
MEMORY	VTR10012, 256k samples/channel in SRAM
	VTR10012-8 with1024 samples/channel in SRAM
TRIGGER/GATE INPUT	TTL Level, Operating mode internally selectable
CLOCK INPUT	TTL Level, 1Mhz minimum, 100Mhz maximum
VME INTERFACE	D16, D32, D32:BLT, A16, A32
CONTROL/STATUS REGISTERS	Read/Write: select clock rate, disarm at cycle completion, bus trigger, external clock, external trigger/gate, reset on trigger, wrap, post, multiple post, pre/post, and multiple pre/post trigger modes, arm, active, channel data addresses, real time trigger addresses, trigger delay,
GATE DURATION REGISTER	Read/Write: select the number of conversions to perform after a trigger.
ADDRESS REGISTER	Read/Write: channel data addresses
REAL TIME ADDRESS	Read real time trigger addresses
TRIGGER DELAY	Read/Write active trigger delay
PRE/POST SELECTION	Read/Write, select number of multiple pre/post cycles
INTERRUPT ID REGISTER	Read/Write Status/ID word
IRQ LEVEL REGISTER	Read/Write IRQ levels
SYSRESET, INT. RESET	Resets module and control register, aborts recording cycle
POWER REQUIREMENTS:	+5V, 2A; -12V, 250ma, 13 watts total at 100Mhz
SIZE:	Single width "VME" 6U card
CONNECTORS	LEMO ERA 00.250
	LEMO ERA 0302, for differential inputs
	SMA connectors optional
OPTIONS	VTR10012-256, 256k samples/channel
	VTR10012-8, 1024 samples/channel
	VTR10012-FP, Front panel real time outputs, 4 channel

JEI0102

PLEASE NOTE: When chosing an analog input module many factors should be considered. It is recommended reading "SELECTING AN ANALOG INPUT MODULE" on our web site: www.joergerinc.com , under "What's New"

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